**CS 1134 : Computer Organization and Architecture**

**Problem Sheet 2 (Not to be submitted but strongly recommended to solve)**

1.Consider a single bus CPU architecture with following registers:

R1,R2,R3 : GPR, MAR, MDR, SP, PC, IR, Internal registers Y & Z.

(a)Write the control signals for the following instructions:

1. MOV R1, [R2] ; copy the contents of location pointed by R2 to Register R1
2. ADD R3, R1, R2 ; Add the contents of register R1 and R2 and store in R3
3. Jump [R1] ; Execute the instruction whose address is stored in R1.

You have to write the instruction fetch signals only for first instruction.

(b) Assuming that the CPU has only these 3 instructions in the instruction set, draw the hard wired control for each control signal.

2. Repeat 1(a) for 2-bus organization where each bus can be used for both input and output.

3. Repeat 1(a) for 3 bus organization as shown in the class.

4. Consider a single bus CPU with

-10 General purpose registers, MAR, MDR, SP, PC, IR, Y, Z

- Memory functions Read and Write

- 14 CPU operations (Add, Sub, mult…….. etc)

- one End signal

Calculate the size of the control word for (a) Horizontal Microprogramming (b) Vertical Microprogramming.

5. Consider a 4 level memory hierarchy system with following specifications:

L1: Size 100 GB, Memory Access time : 100 microsecond, hit rate =1, cost per GB : Rs. 100

L2: Size 1 GB, Memory Access time: 2 microsecond, hit rate : 0.95, cost per GB Rs. 500

L3: Size 100 MB, Memory Access time: 300 Nanosec, hit rate 0.9, cost per MB =Rs.

Size 1 MB, Memory Access time : 1 nanosecond, hit rate : 0.85, Cost per MB : Rs. 500 What is the effective access time and total cost of the memory system?

1. If my budget is only Rs. 5000 and I need minimum 50 GB total memory, what sizes would you suggest for each level of memory system which will give me best effective access time?

6. Consider a memory system with 256 memory blocks (0-255) and 8 cache blocks. If for the execution of a particular program requires memory blocks in following order:

5, 3, 8, 11, 21, 0, 1, 17, 15, 7, 15, 8, 0, 3, 1,237, 18, 5, 0, 8, 15, 7, 5, 3

Draw the cache map for each memory request for

(a) Direct mapping

(b) Fully associative using (i) FIFO (ii) LRU

(c) Two -Way Set Associative cache organizations using (i) FIFO (ii) LRU and calculate the hit ratio. For each miss, tell whether it is a cold miss, capacity miss or conflict miss.